

REMARKS

Applicants respectfully request reconsideration and allowance of the subject application. Claims 1, 3-9, 12, 16-21, 23, 26, 26 and 29-47 are pending in the application.

Allowable Claims

Claims 29-32 would be allowable if a terminal disclaimer were filed to overcome the double patenting rejection. Applicants thank the Examiner for this indication of allowable subject matter. Claims 29-32 remain unchanged and pending in the application. Applicants request that the rejection of Claims 29-32 be held in abeyance pending further examination of the other claims pending in the application.

Claim Rejection under 35 U.S.C. § 102

Claims 1-7 and 9-27 stand rejected under 35 U.S.C. § 102 as being anticipated by “Power Aware Page Allocation” by Lebeck et al. Applicants traverse.

The Lebeck Reference

Lebeck describes an “abstract model” of storing code and data in multiple independently controlled memory chips each having multiple power states. Lebeck discloses that pages of code and data may be stored according to a random placement policy or a sequential placement policy (e.g., sequential first-touch). According to the random placement policy, the operating system randomly chooses a memory chip for storing each page in a memory instruction. According

1 to the sequential placement policy, the operating system sequentially stores the
2 pages of a memory instruction in a given memory chip until the entire chip is
3 filled before moving on to the next chip. Both random and sequential placement
4 policies are performed at the time that the content is first saved in the physical
5 memory. Lebeck teaches that if a sequential placement policy is utilized, the
6 contents in the physical memory may be reorganized one time to cluster the most
7 frequently accessed pages in a particular memory chip (e.g., frequency placement
8 policy). Finally, Lebeck discloses that each (e.g., dynamic power management
9 policy) or all (e.g., static power management policy) of the memory devices are set
10 to a reduced power mode after a static threshold period of time from the last
11 memory access.

12 13 Claim 1

14 Claim 1, as amended, recites “creating mappings from received addresses
15 to physical memory by a hardware interface disposed between a processor and a
16 number of physical memory devices” and “modifying the mappings by the
17 hardware interface . . .” Lebeck does not teach or suggest that mappings are
18 created or modified at a hardware interface disposed between a processor and the
19 physical memory devices. Instead, Lebeck discloses that a reassignment is
20 performed by the operating system. Specifically, Lebeck teaches “the OS sorts the
21 counters and performs the movement and repacking operations, and resumes
22 program operation,” section 6.3. Since the OS is executed by the processor, it is
23 clear that Lebeck’s processor itself performs reassignment.

24 Thus, Lebeck does not disclose that the mappings are created and modified
25 at a hardware interface disposed between a processor and the physical memory

1 devices. Therefore Applicants respectfully submit that Claim 1 is patentable over
2 Lebeck. Applicants respectfully request that the §102(a) rejection of Claim 1 be
3 withdrawn and Claim 1 be allowed.
4

5 Claims 2 and 39-47

6 Dependent Claims 39-47 are allowable by virtue of their dependency on
7 respective base Claim 1, as well as the additional elements they recite. With
8 respect to Claim 39, the additional elements include “receiving memory
9 instructions from a processor or graphics adapter by the hardware interface.”
10 Lebeck does not teach or suggest that the memory instruction are received by a
11 hardware interface that is disposed between the processor and the memory.
12 Accordingly, those skilled in the art would appreciate that the systems and
13 methods of Lebeck would not permit memory access by other sources such as a
14 graphics adapter. Accordingly, Applicants respectfully submit that Claim 39
15 contains elements that are not disclosed by Lebeck and therefore is patentable over
16 Lebeck.
17

18 With respect to Claim 40, the additional elements include that “the
19 mappings are modified at the hardware interface independently of the operation
20 system”. To the extent that Lebeck teaches that the mappings may be modified,
21 Lebeck discloses that the mappings are modified by the operation system, section
22 6.3. Accordingly, Applicants respectfully submit that Claim 40 contains
23 limitations that are not disclosed by Lebeck and therefore is patentable over
24 Lebeck.
25

1 With respect to Claim 41, the additional limitations include “refreshing the
2 content of physical memory devices by the hardware interface independently of
3 the operating system.” Those skilled in the art appreciate that, because the
4 mappings are created and modified by a hardware interface between the processor
5 and the memory, the memory may be refreshed independently of the operating
6 system. However, Lebeck discloses that the mappings are created and modified
7 by the operating system. Therefore, the systems and methods of Lebeck do not
8 permit refreshing the content of the memory device independently of the operating
9 system. Accordingly, Applicants respectfully submit that Claim 41 contains
10 limitations that are not disclosed by Lebeck and therefore is patentable over
11 Lebeck.

12
13 With respect to Claim 42, the additional limitations include “identifying
14 one or more of the plurality of memory devices referenced by relatively few
15 mappings” and “setting the identified one or more of the plurality of memory
16 devices to a reduced power state.” Lebeck does not teach or suggest identifying
17 one or more of the plurality of memory device referenced by relatively few
18 mappings. Instead, Lebeck discloses identifying frequently accessed pages. The
19 frequency of mappings is different from the frequency with which pages are
20 accessed. Lebeck also does not teach or suggest setting the memory devices,
21 identified as a function of the frequency of mappings thereto, to a reduced power
22 state. Instead, Lebeck discloses that pages are reassigned as a function of page
23 access frequency, section 4. Furthermore, Lebeck discloses that a reduced power
24 state of a given memory device is entered after a threshold period of time has
25 expired from the last access to the given memory device. Accordingly, Applicants

1 respectfully submit that Claim 42 contains elements that are not disclosed by
2 Lebeck and therefore is patentable over Lebeck.

3
4 With respect to Claim 43, the additional limitations include “re-mapping
5 the identified portions of the processor’s physical address space to physical
6 memory by the hardware interface in a manner that reduces the number of
7 physical memory devices referenced by the identified portions of the processor’s
8 physical address space.” Lebeck does not teach that the remapping is done at a
9 hardware interface. Instead, Lebeck discloses that reassignment is performed by
10 the operating system. Accordingly, Applicants respectfully submit that Claim 43
11 contains elements that are not disclosed by Lebeck and therefore is patentable over
12 Lebeck

13
14 With respect to Claim 44, the additional limitations include that “the re-
15 mapping is periodically performed after a pre-defined number of memory
16 references.” To the extent that Lebeck may teach re-mapping the logical address
17 space to the physical address space, Lebeck discloses that the re-mapping is
18 performed one time, section 4. With respect to Claim 45, the additional
19 limitations include that “the re-mapping is performed after power consumption by
20 the physical memory reaches a determined threshold.” Lebeck does not teach or
21 suggest re-mapping the logical address space to the physical address space after
22 power consumption by the physical memory reaches a determined threshold. With
23 respect to Claim 46, the additional limitations include that “the re-mapping is
24 periodically performed after a pre-defined number of memory allocations.” To the
25 extent that Lebeck may teach re-mapping the logical address space to the physical

1 address space, the re-mapping is unrelated to the allocation status of memory.
2 With respect to Claim 47, the additional limitations include that “the re-mapping is
3 performed at periodic time intervals.” To the extent that Lebeck may teach re-
4 mapping the logical address space to the physical address space, Lebeck discloses
5 that the re-mapping is performed one time, section 4. Applicants respectfully
6 submit that Claims 44, 45, 46 and 47 each contain elements that are not disclosed
7 by Lebeck and therefore are patentable over Lebeck.

8
9 For the above-advanced reasons, Applicants assert that Claims 2 and 39-47
10 are patentably distinguishable over Lebeck. Accordingly, Applicants respectfully
11 request that the §102(a) rejection of Claims 2 and 39-47 be withdrawn and Claims
12 2 and 39-47 be allowed.

13
14 Claim 3

15 Claim 3, as amended, recites “a memory controller” comprising “means for
16 receiving memory instructions from a processor . . .”. Claim 3 has been rejected
17 as being anticipated by Lebeck. However, as already discussed above, to the
18 extent that Lebeck performs reassignment, such reassignment is performed by the
19 processor itself. Lebeck does not show a memory controller that receives
20 addresses from a processor and that also includes “means for mapping . . .” as also
21 recited by claim 3. Accordingly, Lebeck does not disclose each and every element
22 of claim 3, and the §102 rejection of claim 3 is therefore unfounded. Allowance
23 of claim 3 is therefore requested.

24
25 Claims 4-9, 12, 16, 37 and 38

1 Dependent Claims 4-9, 12, 16, 37 and 38 are allowable by virtue of their
2 dependency on respective base Claim 3, as well as the additional elements they
3 recite. Allowance of these claims is respectfully requested.

4
5 Claim 17

6 Claim 17, as amended, recites “monitoring memory accesses received from
7 a processor to identify portions of the processor’s address space based on usage “
8 and “periodically re-mapping the processor’s address space to physical memory to
9 reduce the number of physical memory devices referenced by the identified
10 portions of the processor’s address space.” As already discussed, to the extent that
11 Lebeck performs reassignment of physical memory, such reassignment is done by
12 the processor itself. Lebeck describes no process in which memory instructions
13 are received from a processor and remapped at that point to physical memory.
14 Accordingly, Lebeck does not show each and every element of claim 17, and
15 claim 17 should therefore be allowed.

16
17 Claims 18-21, 23, 25 and 37

18 Dependent Claims 18-21, 23 and 25 are allowable by virtue of their
19 dependency on respective base Claim 17, as well as the additional elements they
20 recite. Accordingly, Applicants respectfully request that the §102(a) rejection of
21 Claims 18-21, 23 and 25 be withdrawn and Claim s18-21, 23 and 25 be allowed.

22
23 Claim 26

24 Claim 26, as amended, recites a “memory controller configured to map
25 allocated portions of the logical address space to corresponding portions of

1 physical address space in a manner that tends to reduce the number of physical
2 memory devices referenced by the allocated portions of the logical address space”
3 and “the memory controller further configured to move portions of memory
4 regions corresponding to allocated portions of the logical address space in
5 response to identification of de-allocated portion of the logical address space and
6 re-mapping the corresponding portions of the physical address space and
7 corresponding portion of the logical address space to reduce the number of
8 physical memory devices referenced by allocated portion of logical memory.”
9 Applicants respectfully assert that Lebeck does not teach or suggest allocating
10 memory in a manner that tends to reduce the number of physical memory device
11 referenced by the allocated portion of the logical address space. Instead, Lebeck
12 discloses storing pages in memory in a manner that tends to reduce the number of
13 physical memory devices. Storing pages in memory and allocating memory are
14 not equivalent. Lebeck also does not teach or suggest moving portion of the
15 logical address space when memory is de-allocated and re-mapping the
16 corresponding portions to reduce the number of physical memory devices
17 referenced. Instead, Lebeck discloses reassigning memory based upon the
18 frequency at which the stored pages are accessed.

19
20 For the above-advanced reasons, Lebeck does not teach or suggest a
21 “memory controller configured to map allocated portions of the logical address
22 space to corresponding portions of physical address space in a manner that tends
23 to reduce the number of physical memory devices referenced by the allocated
24 portions of the logical address space” or “the memory controller further
25 configured to move portions of memory regions corresponding to allocated

1 portions of the logical address space in response to identification of de-allocated
2 portion of the logical address space and re-mapping the corresponding portions of
3 the physical address space and corresponding portion of the logical address space
4 to reduce the number of physical memory devices referenced by allocated portion
5 of logical memory.” Therefore Applicants respectfully submit that Claim 26 is
6 patentable over Lebeck. Applicants respectfully request that the §102(a) rejection
7 of Claim 26 be withdrawn and Claim 26 be allowed

8
9 Claims 33-36

10 Dependent Claims 33-36 are allowable by virtue of their dependency on
11 respective base Claim 26, as well as the additional elements they recite.
12 Accordingly, Applicants respectfully request that the §102(a) rejection of Claims
13 33-36 be withdrawn and Claims 33-36 be allowed.

14
15 Claim Rejection under 35 U.S.C. § 103

16 Claims 8 stands rejected under 35 U.S.C. § 103 as being obvious in view of
17 “Power Aware Page Allocation” by Lebeck et al., “Optimizing the DRAM
18 Refresh Count for Merged DRAM/Logic LSIs” by Ohsawa and U.S. Patent
19 6,167,484 to Boyer. Dependent Claim 8 is allowable by virtue of its dependency
20 on respective base Claim 3. Accordingly, Applicants respectfully request that the
21 §103(a) rejection of Claim 8 be withdrawn and Claim 8 be allowed.

- 1
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 17
- 18
- 19
- 20
- 21
- 22
- 23
- 24
- 25

- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 17
- 18
- 19
- 20
- 21
- 22
- 23
- 24
- 25

8

9

1

10

11

1

12